KONERU LAKSHMAIAH EDUCATION FOUNDATION

(Deemed to be University, Estd. u/s. 3 of UGC Act 1956)

B.Tech - Even Sem : End Semester Exam

Academic Year:2021-2022

19CS3251R - Advanced Computer Architecture

Set No: 3

Time: | **Max.Marks: 100**

Answer All Questions

S.NO		Choice	Options	Marks	CO	CO BTL	COI BTL
1.	Differentiate MIPS and 80x86 processors based on the types and sizes of operands	choice Q-2		10Marks	CO1	2	1
2.	Define CPU execution time, user CPU time, system CPU time and write the expression for the CPU time			10Marks	CO1	2	2
3.	Answer the Following	choice Q-4		15Marks	CO1	2	1
3.A.	Differentiate between the primary and secondary storage devices and explain in detail about the different secondary storage devices			8Marks	CO1	2	1
3.B.	How does the compiler know which code to compile for CPU and which one for GPU			7Marks	CO1	2	2
4.	Answer the Following			15Marks	CO1	2	2
4.A.	Define Latency and throughput of a computer system			7Marks	CO1	2	2
4.B.	State the Amdahl's law, define speedup and derive the speedup equation			8Marks	CO1	2	2
5.	Discuss in detail major hurdles in pipelining.	choice Q-6		10Marks	CO2	2	1
6.	List the primary components of instruction Set Architecture of VMIPS and briefly explain them			10Marks	CO2	2	2
7.	Answer the Following	choice Q-8		15Marks	CO2	2	1
7.A.	Explain dynamic scheduling using Tomosulo's approach with an example			8Marks	CO2	2	1
7.B.	Demonstrate the concepts of ILP with various types of dependencies in ILP with examples			7Marks	CO2	2	1
8.	Answer the Following			15Marks	CO2	2	2
8.A.	Differentiate RISC and CISC architectures			8Marks	CO2	2	2
8.B.	Explain in detail about Graphics Processing Units and its Programming			7Marks	CO2	2	2
9.	Explain Dynamic Scheduling? Explain how it is used to reduce data hazard.	choice Q-10		10Marks	CO3	3	1
10.	Explain RAID architecture in detail with its various levels			10Marks	CO3	3	2
11.	Answer the Following	choice Q-12		15Marks	CO3	3	2
11.A.	Explain the snoopy based Cache coherence protocols with neat diagram			8Marks	CO3	3	2
11.B.	List out the advantages of CMP architecture?			7Marks	CO3	3	2
12.	Answer the Following			15Marks	CO3	3	3
12.A.	Explain the basic architecture of a distributed memory multiprocessor system			8Marks	CO3	3	2
12.B.	Explain in detail about CMP and SMT architecture and its performance			7Marks	CO3	3	3
13.	Explain the trends in Cost, Price for building computer over time	choice Q-14		10Marks	CO4	4	1
14.	Explain the Tournament Branch predictors in detail.			10Marks	CO4	4	2
15.	Answer the Following	choice Q-16		15Marks	CO4	4	2
15.A.	Discuss in detail about various hit time reduction techniques to improve cache performance			7Marks	CO4	4	2
15.B.	Define memory access time and give the equations to calculate Average memory access time2-way and Average memory access time4-way			8Marks	CO4	4	2
16.	Answer the Following			15Marks	CO4	4	2
16.A.	With examples, explain how do you detect and enhance Loop Level Parallelism?			8Marks	CO4	4	3
16.B.	List the methods for providing synchronization in threads?			7Marks	CO4	4	3

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